REMARKS

Reconsideration of the application is respectfully requested.

The following discussion addresses the issues in the order in which they have been raised in the Office Action.

Claim Objections

The Office Action indicates that claims 7-9 contain objectionable language in the form of "the current data". This has been alleviated in the amendment here without narrowing the scope of the claims. As to the suggestion for clarifying claims 1,9, 10 and 19, by replacing "if" with -- when --, this has also been adopted as seen in the amendment here.

Claims Rejected Under 35 U.S.C. §112

The Office Action has rejected claim 10 as having improper antecedent basis for "the current content". In response, Applicants have taken this opportunity to clarify such claim language in claim 10, as well as in several other claims. These clarifications are not intended to be narrowing.

Claims Rejected Under 35 U.S.C. §103

The claims stand rejected as being obvious over U.S. Patent No. 6,185,696 issued to Noll ("Noll") in view of U.S. Patent No. 6,757,838 issued to Chaiken, et al. ("Chaiken"). Applicants respectfully disagree with the rejection for the following reasons.

According to the Office Action, Noll discloses *nonvolatile data storage devices to store CMOS BIOS data and a mirror image of such data,* pointing to Fig. 1, reference numerals 22, 30, and col. 2, lines 40-43. Those sections of Noll refer to BIOS code, while Applicants' claim language *CMOS BIOS data* refers to a type of configuration data traditionally referred to as **CMOS memory data**, not BIOS code. This has been corrected in the amendment here.

The difference between CMOS memory data and BIOS code, as understood by one of ordinary skill in the art, is as follows: CMOS memory data is certain known configuration data that, in the early days of personal computers, was stored in a battery backed up CMOS integrated circuit device (the term "CMOS" has been kept over the years). This configuration data changes each time a computer is turned on and booted. The CMOS data is used to configure a system for boot, while BIOS code (or simply, BIOS) consists of the actual instructions that boot the system. See also the attached printout ("The PC Guide", BIOS CMOS Memory, Site Version 2.2.0 – version Date: April 17, 2001 [http"//www.pcguide.com/ref/mbsys/bios/compCMOS-c.html], 3 pages) and "What's the Difference Between BIOS and CMOS?", University Information Technology Services, Knowledge Base, Indiana University (last modified 12/23/2005), both obtained from the Web, confirming this understanding of those of ordinary skill.

The above distinction between CMOS data and BIOS code is also apparent in the references relied upon in the art rejection. In Noll, while most of the discussion refers to the BIOS and its backup copy, col. 8 has a good discussion that illustrates the difference between CMOS and BIOS. In Chaiken, the discussion about primary and secondary BIOS also includes a brief but instructive portion on CMOS RAM which "is used to store configuration data for the computer ..." (Chaiken, col. 2 lines 54-57.) In Chaiken, see also col. 7, lines 31-44 which further illustrates the distinction between CMOS and BIOS in the context of the invention.

While Noll and Chaiken refer to BIOS code being duplicated and restored, neither reference teaches or suggests Applicants' claims 1 and 10 as amended here, and in particular a first device to store CMOS memory data, wherein the first device lacks hardware security such that the CMOS memory data storage regions are modifiable by an application program on the system, a second device to store a mirror image of the CMOS memory data in a location that cannot be modified without system authorization, and wherein validity of the CMOS memory data stored in the first device is ascertained and, when invalid, the data in the first device is replaced with the stored mirror image from the second device.

In addition, the Office Action points to Chaiken, col. 9, line 63 to col. 10 line 4 as allegedly teaching Applicants' claimed *first data storage device that lacks hardware security*

... Applicants respectfully disagree, because Chaiken only considers the situation where a BIOS ROM device **fails** for whatever reason; Chaiken does not contemplate the BIOS ROM device as having an error caused by an unauthorized or improper access from an application program running in the system. Chaiken, col. 2, lines 37-43 and col. 4, lines 1-9. Also, the Office Action's reliance on col. 2, line 59 to col. 3, line 4 for teaching such a device is improper, because that section of Chaiken refers to a CMOS RAM device, while the obviousness rejection actually relies on Chaiken's BIOS ROM as being Applicants' *first storage device*. Accordingly, the rejection of claims 1 and 10 is improper for all of the above reasons.

As to claim 17, neither Noll or Chaiken teaches or suggests generating an integrity metric corresponding to valid CMOS memory content stored in a first region of a first device, and storing the integrity metric in another storage device of the system to later determine when the content in the first region has been modified without authorization. Noll and Chaiken refer to verification of BIOS code, but do not teach or suggest the specific method in claim 17 involving the generation and storage within a system of an integrity metric for CMOS memory data of the system.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the reasons given above in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper in view of the relied upon art reference, and to correct obvious errors in the claims, without altering their scope. A Notice of Allowance referring to claims 1-4, and 6-19, as amended here, is therefore requested to be issued at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account

No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: April 23, 2007

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CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on April 23, 2007.

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Margaux Rodriguez *April 23, 2007*